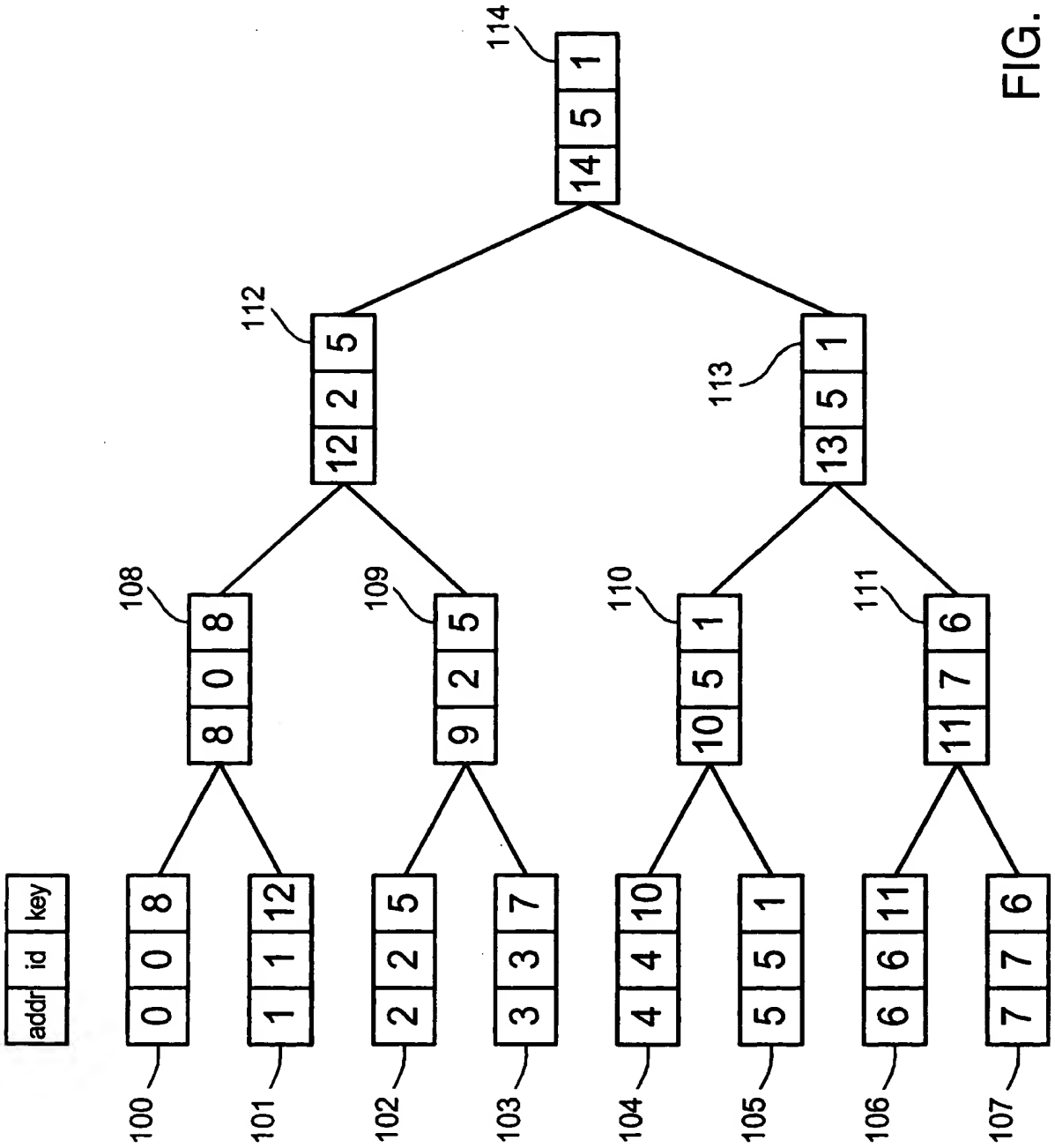
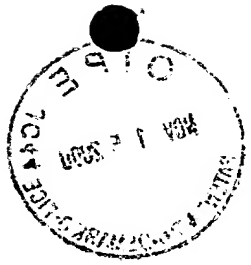

addr
id
key
114
14 5 1
112
12 2 5
113
13 5 1
108
8 0 8
109
9 2 5
110
10 5 1
111
11 7 6
0 0 8
1 1 12
2 2 5
3 3 7
4 4 10
5 5 1
6 6 11
7 7 6
100
101
102
103
104
105
106
107

FIG. 1



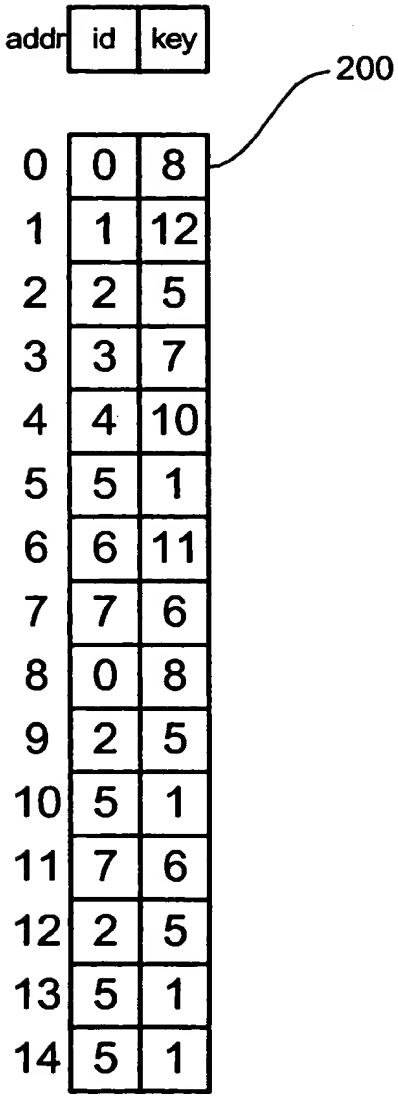

addr
id
key
200
0 0 8
1 1 12
2 2 5
3 3 7
4 4 10
5 5 1
6 6 11
7 7 6
8 0 8
9 2 5
10 5 1
11 7 6
12 2 5
13 5 1
14 5 1

FIG. 2

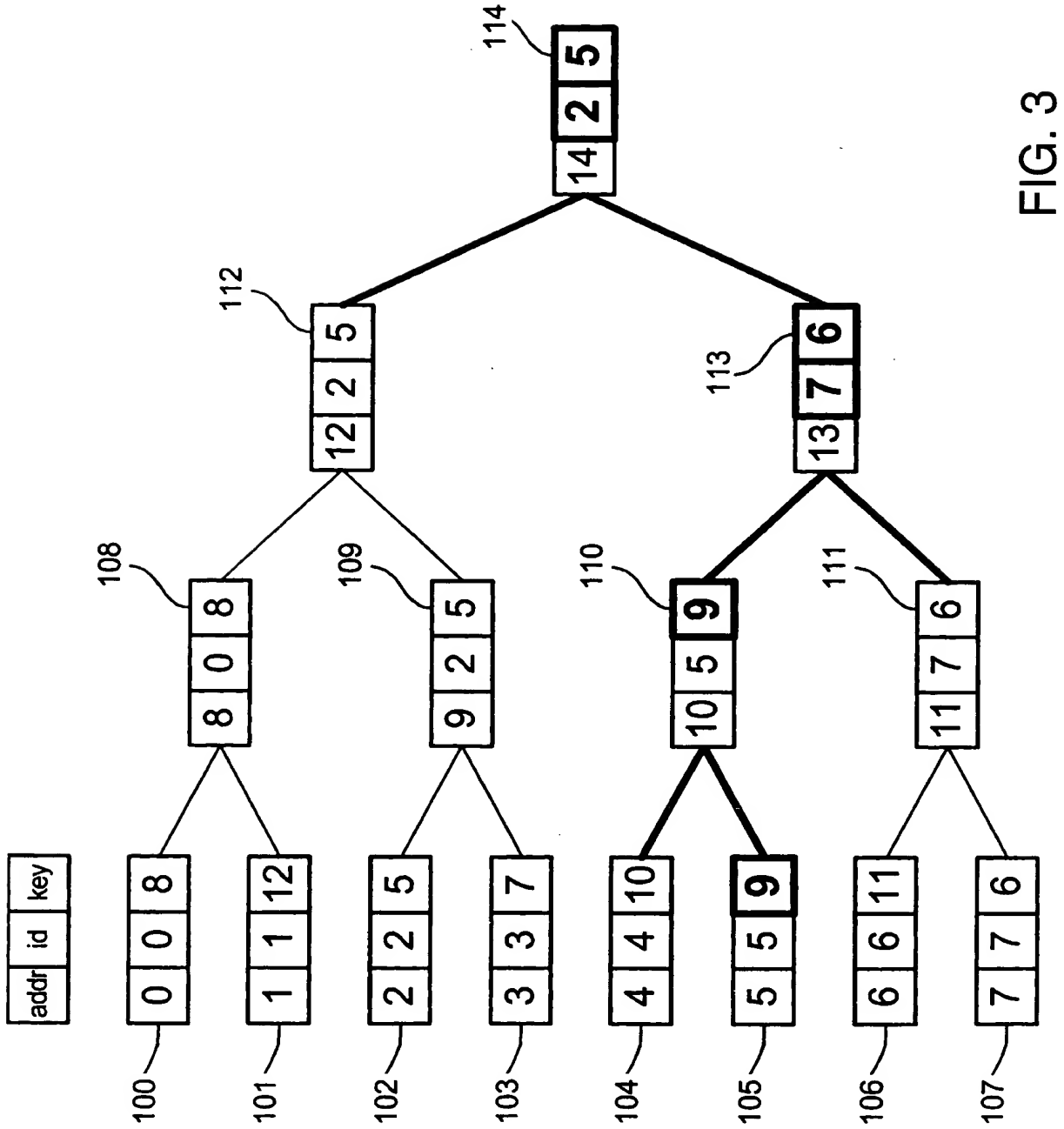

addr
id
key
114
14
2
5
112
12
2
5
113
13
7
6
108
8
0
8
109
9
2
5
110
10
5
9
111
11
7
6
0
0
8
1
1
12
2
2
5
3
3
7
4
4
10
5
5
9
6
6
11
7
7
6
100
101
102
103
104
105
106
107

FIG. 3

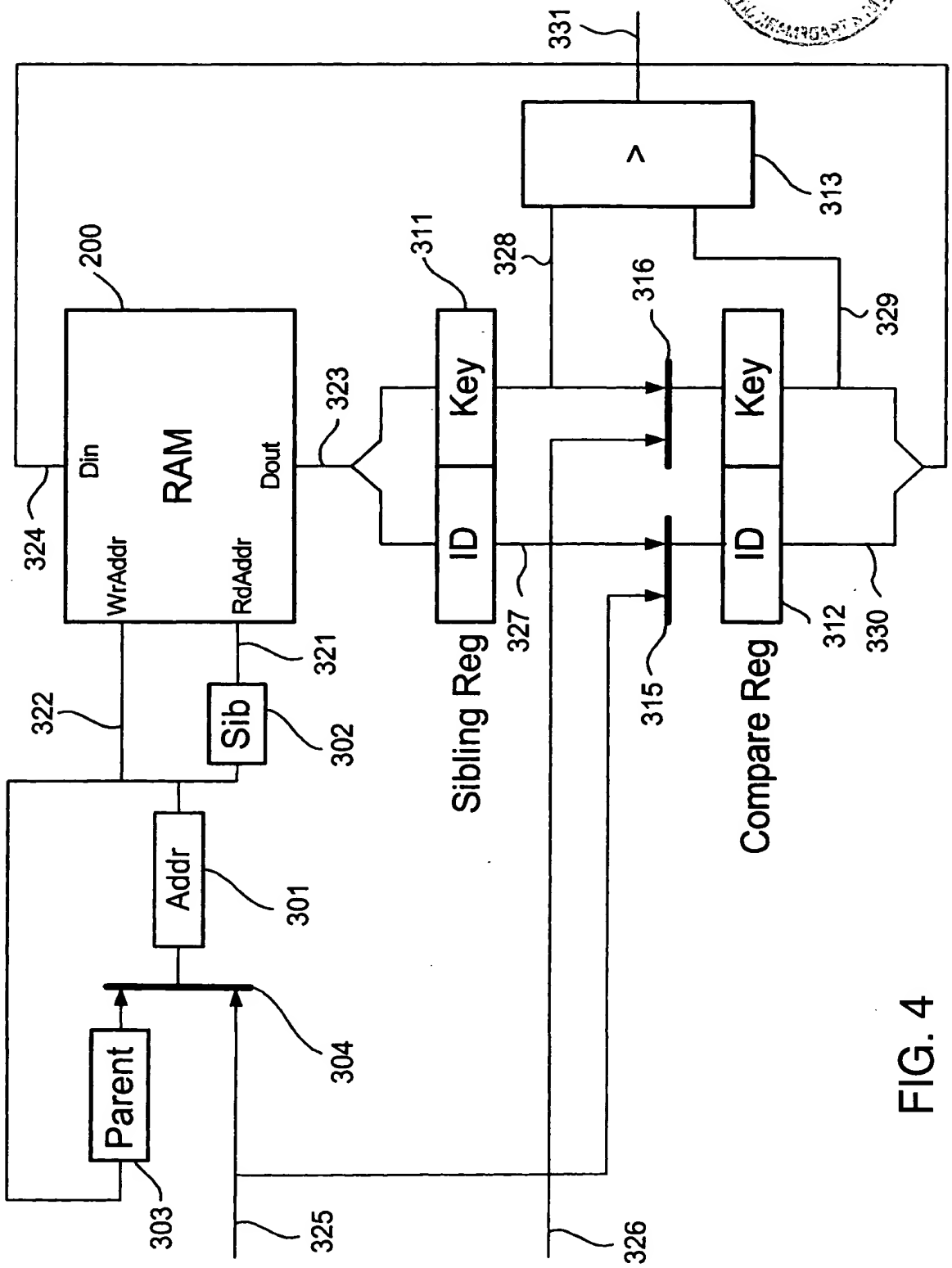

331
>
313
200
311
328
316
329
RAM
Din
Dout
WrAddr
RdAddr
Key
ID
323
324
321
322
Sib
302
Addr
301
Parent
303
304
325
Sibling Reg
327
315
Compare Reg
312
330
326

FIG. 4

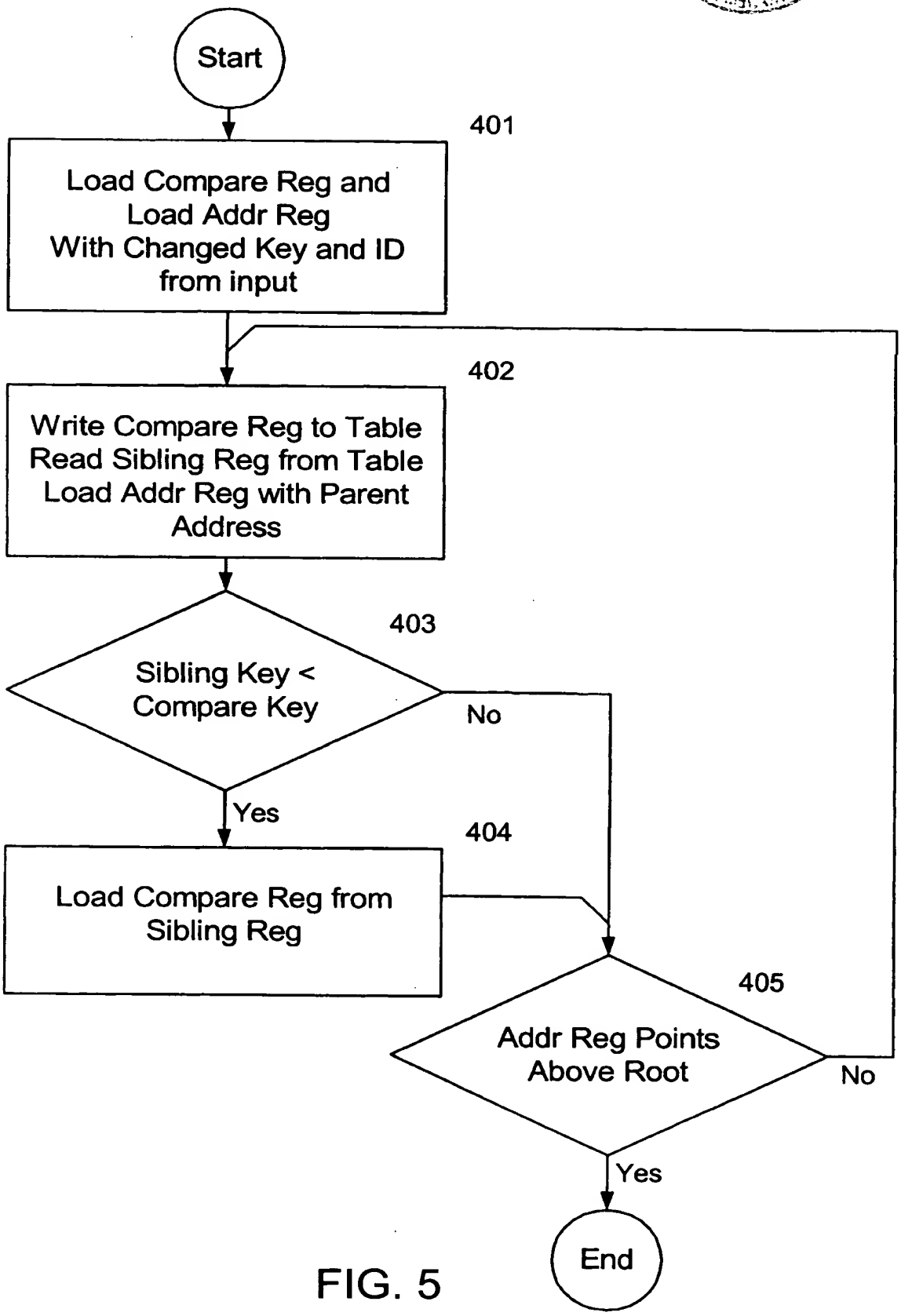

Start
401
Load Compare Reg and
Load Addr Reg
With Changed Key and ID
from input
402
Write Compare Reg to Table
Read Sibling Reg from Table
Load Addr Reg with Parent
Address
403
Sibling Key <
Compare Key
No
Yes
404
Load Compare Reg from
Sibling Reg
405
Addr Reg Points
Above Root
No
Yes
End

FIG. 5

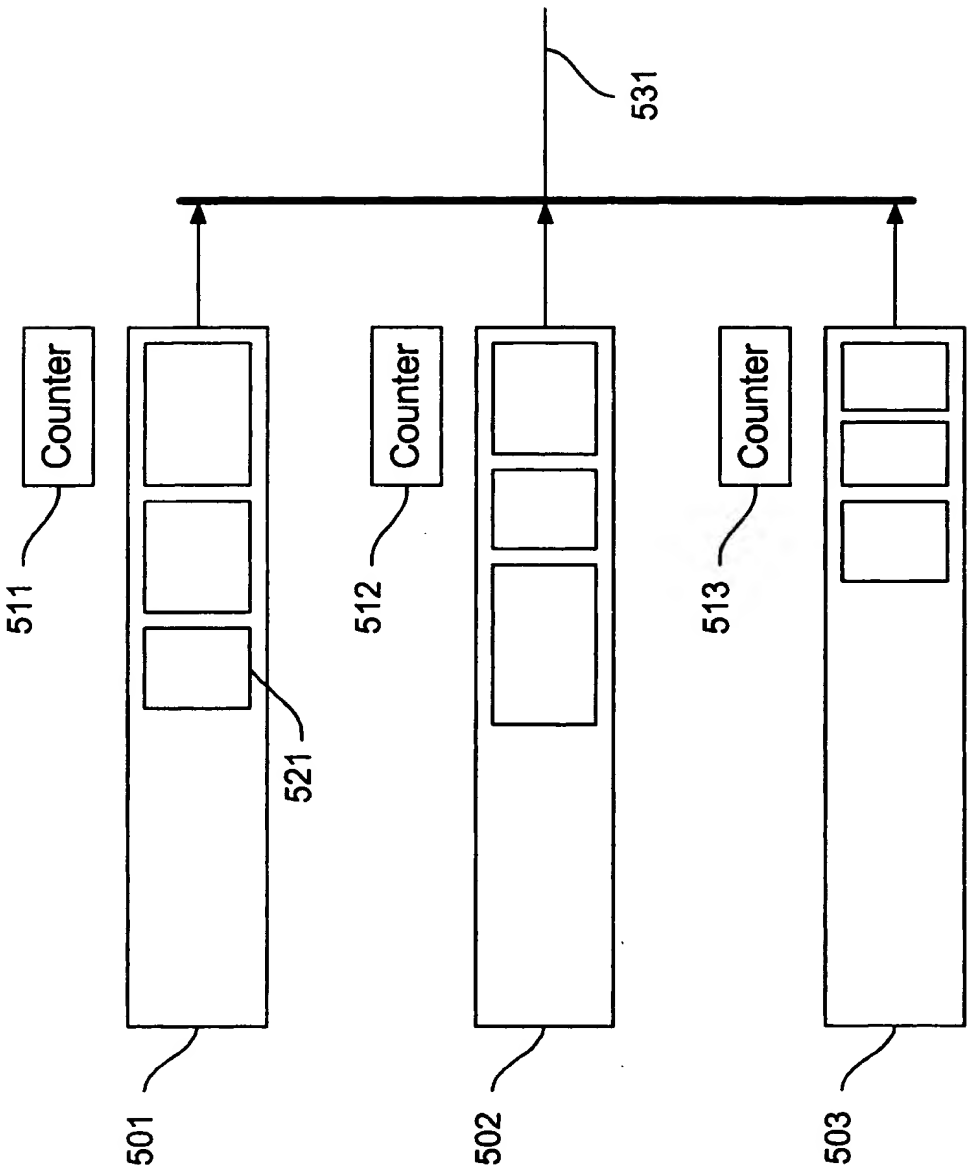


FIG. 6
PRIOR ART

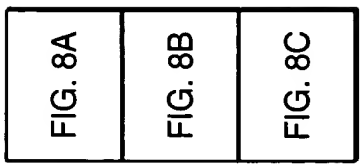


FIG. 8A
FIG. 8B
FIG. 8C

FIG. 8

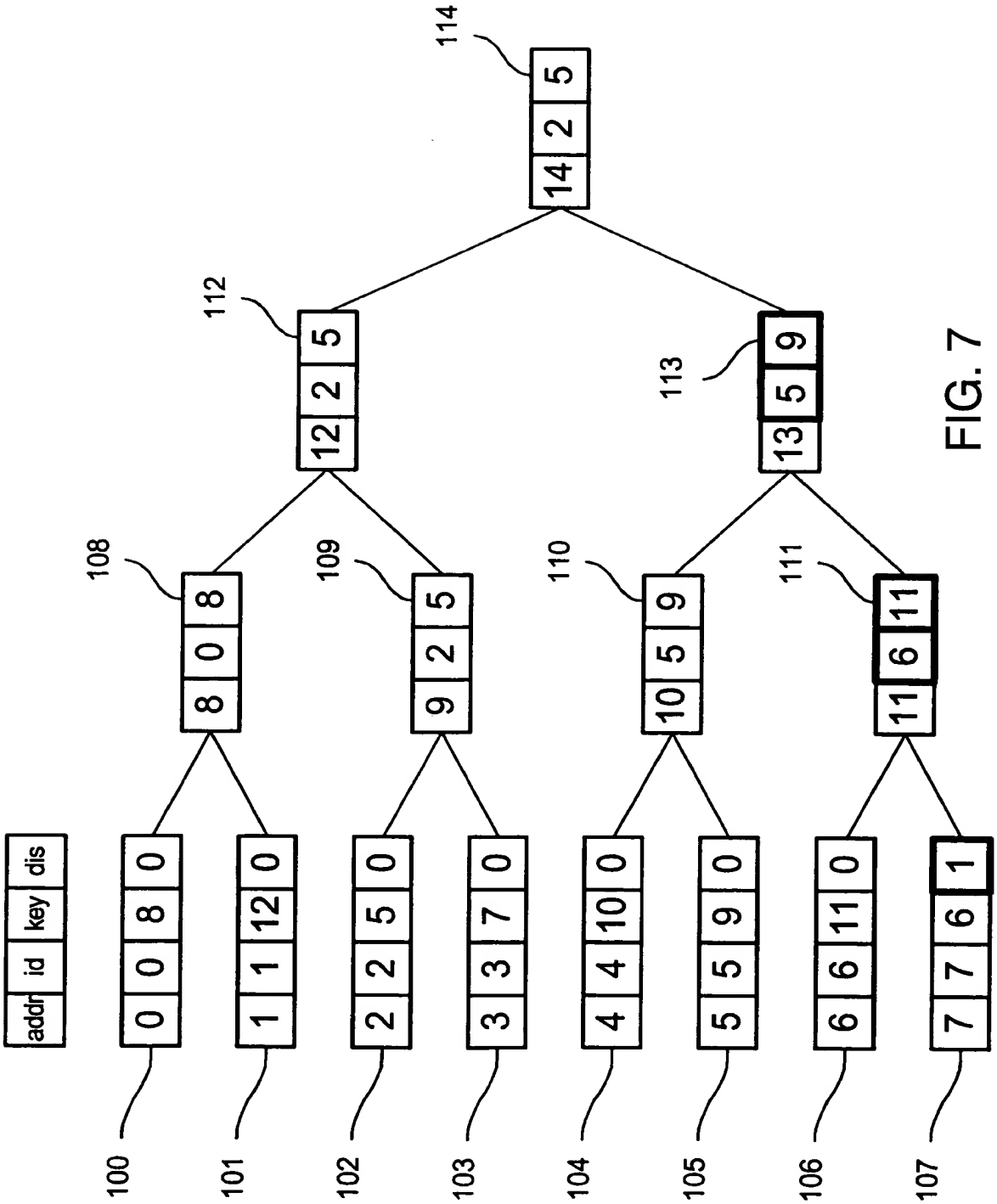

addr
id
key
dis
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114

FIG. 7

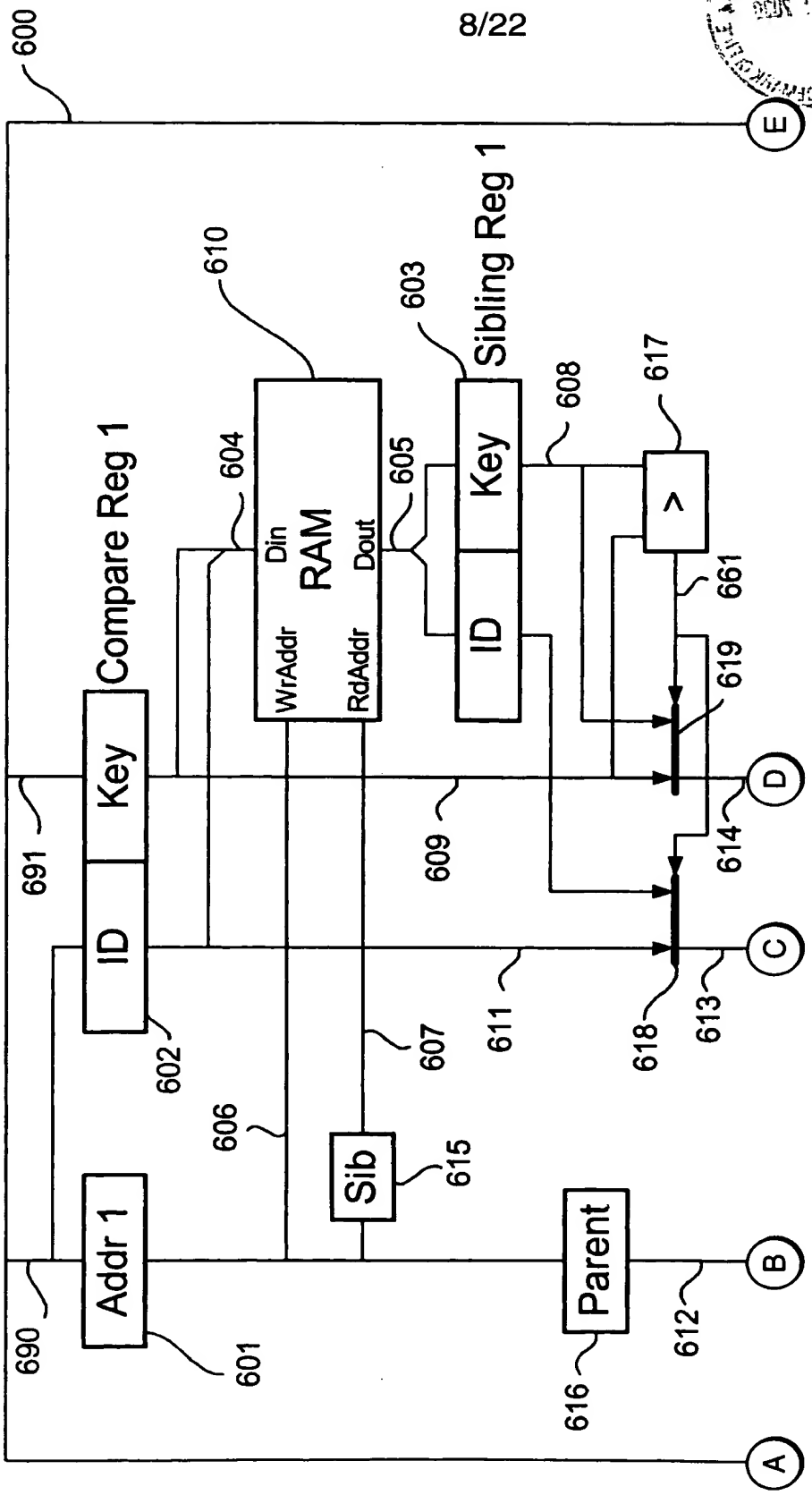

600
E
Sibling Reg 1
603
610
Compare Reg 1
604
Din
RAM
Dout
605
Key
608
617
>
661
ID
619
WrAddr
RdAddr
Key
691
609
614
D
ID
602
607
611
618
613
C
606
Sib
615
Addr 1
690
601
Parent
612
B
616
A

FIG. 8A

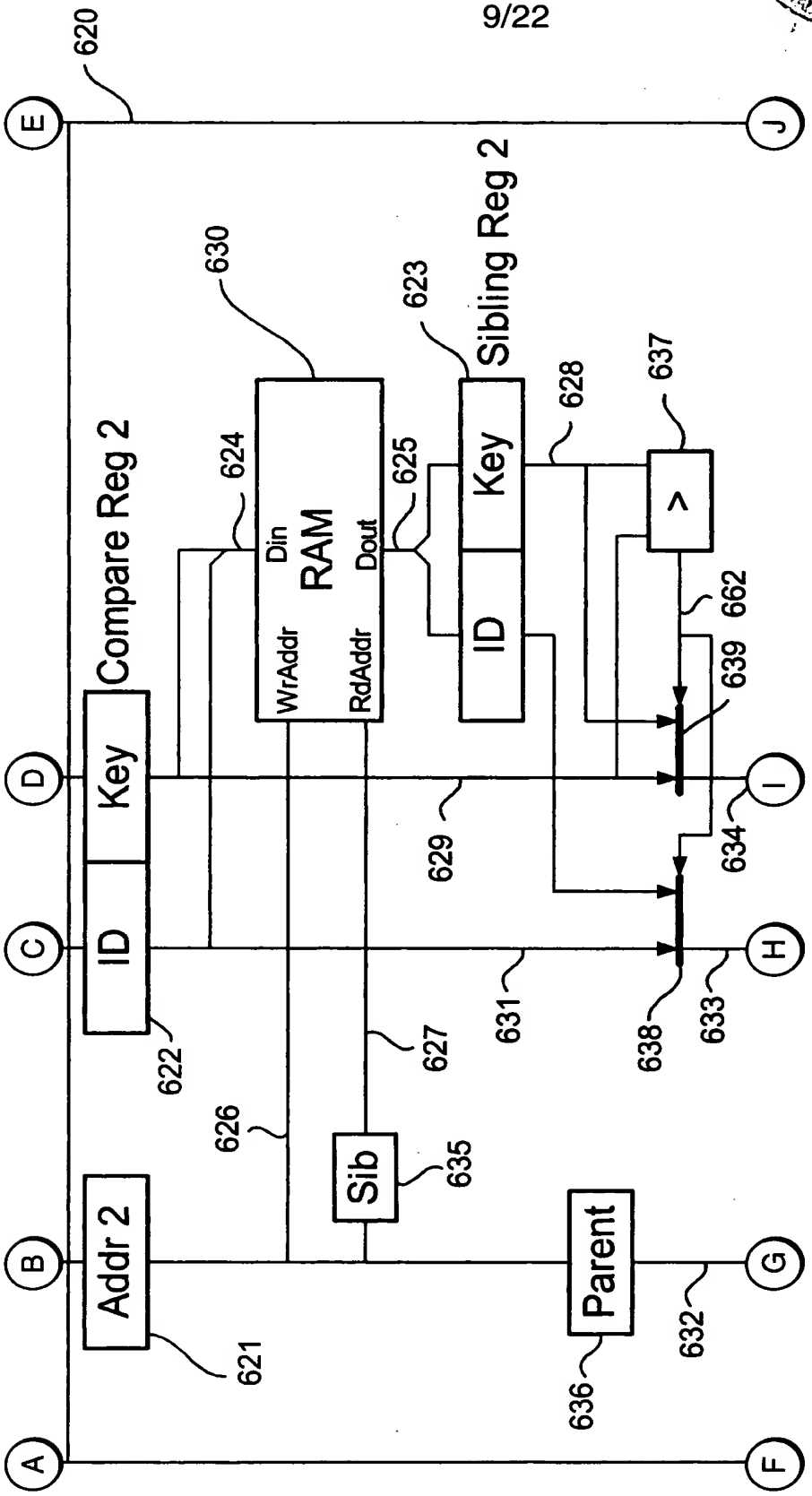

620
E
J
Compare Reg 2
Key
ID
630
624
Din
RAM
WrAddr
RdAddr
Dout
625
623
Sibling Reg 2
Key
ID
628
637
>
662
639
D
I
C
H
629
634
631
638
633
622
627
626
Sib
635
B
G
Addr 2
621
Parent
636
632
A
F

FIG. 8B

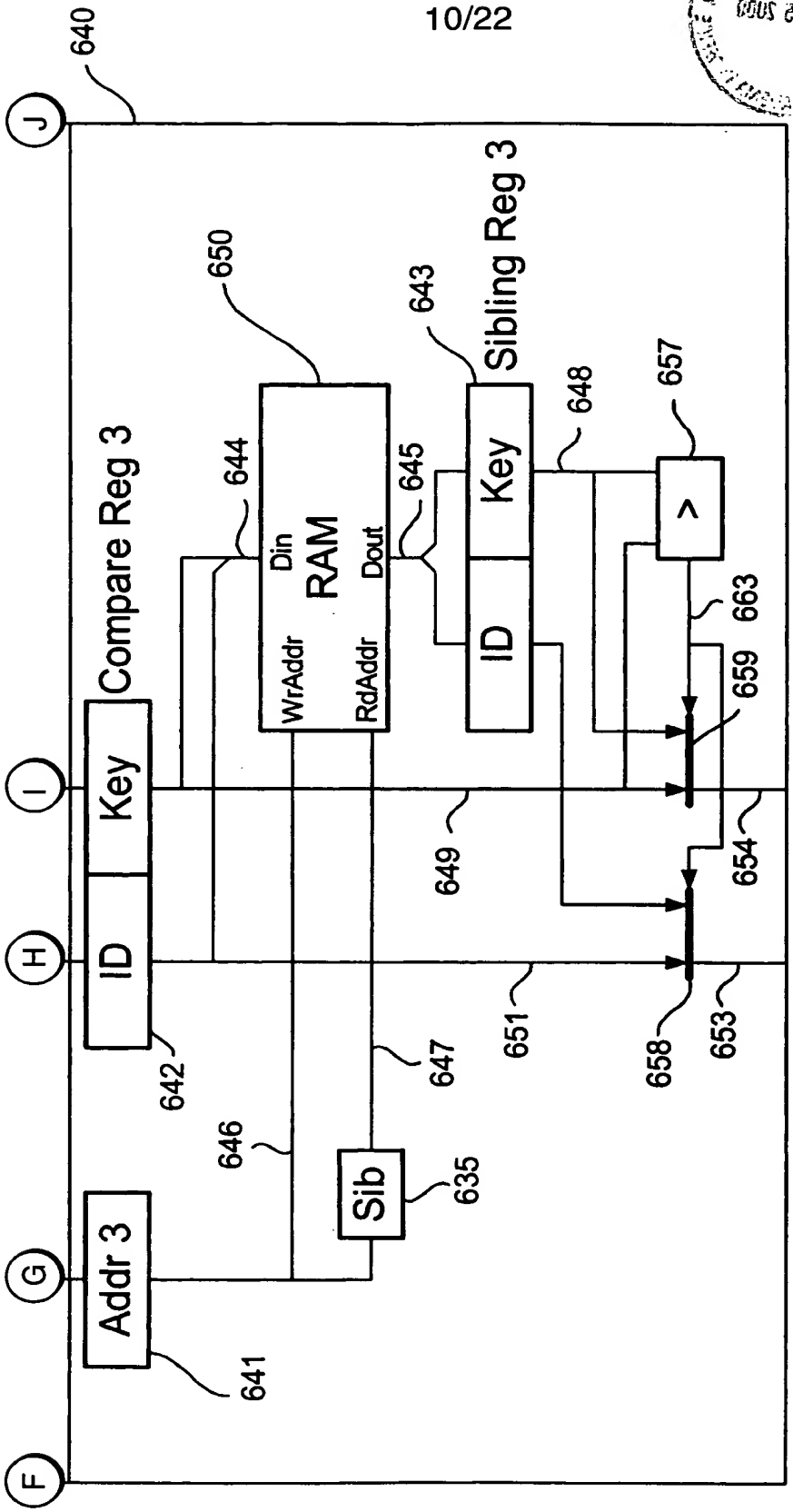

640
J
I
H
G
F
Compare Reg 3
Key
ID
Addr 3
641
642
644
650
Din
RAM
Dout
WrAddr
RdAddr
643
Sibling Reg 3
Key
ID
645
646
647
Sib
635
648
649
651
657
>
663
659
654
658
653

FIG. 8C

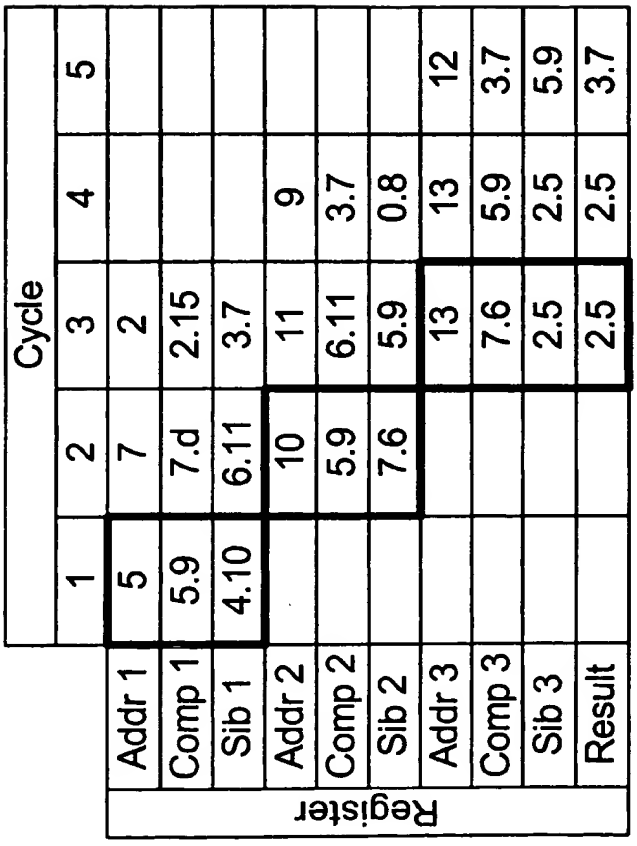

Cycle
1
2
3
4
5
Register
Addr 1
5
7
2
Comp 1
5.9
7.d
2.15
Sib 1
4.10
6.11
3.7
Addr 2
10
11
9
Comp 2
5.9
6.11
3.7
Sib 2
7.6
5.9
0.8
Addr 3
13
12
Comp 3
7.6
5.9
3.7
Sib 3
2.5
2.5
5.9
Result
2.5
2.5
3.7

FIG. 9

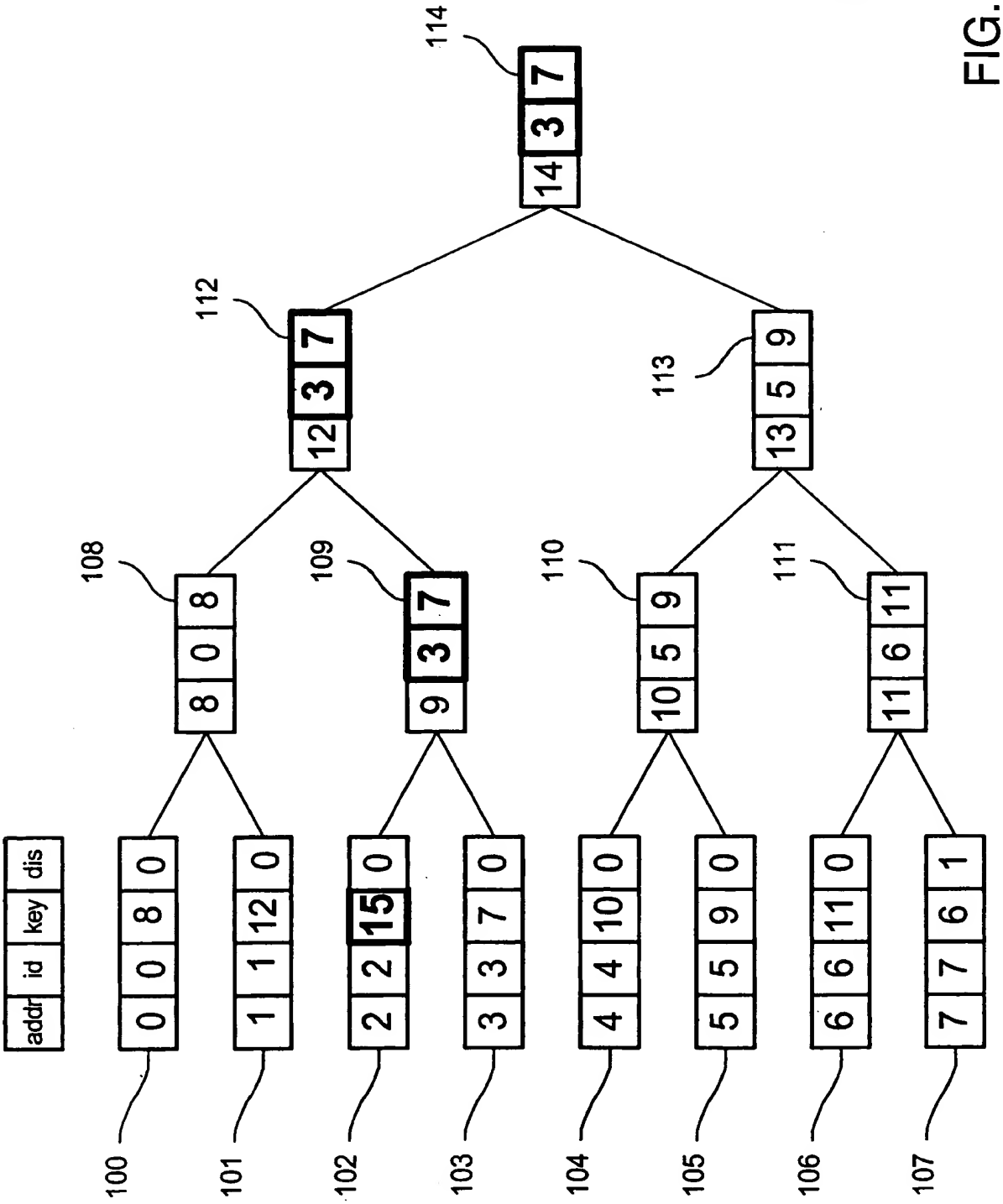

addr
id
key
dis
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114

FIG. 10

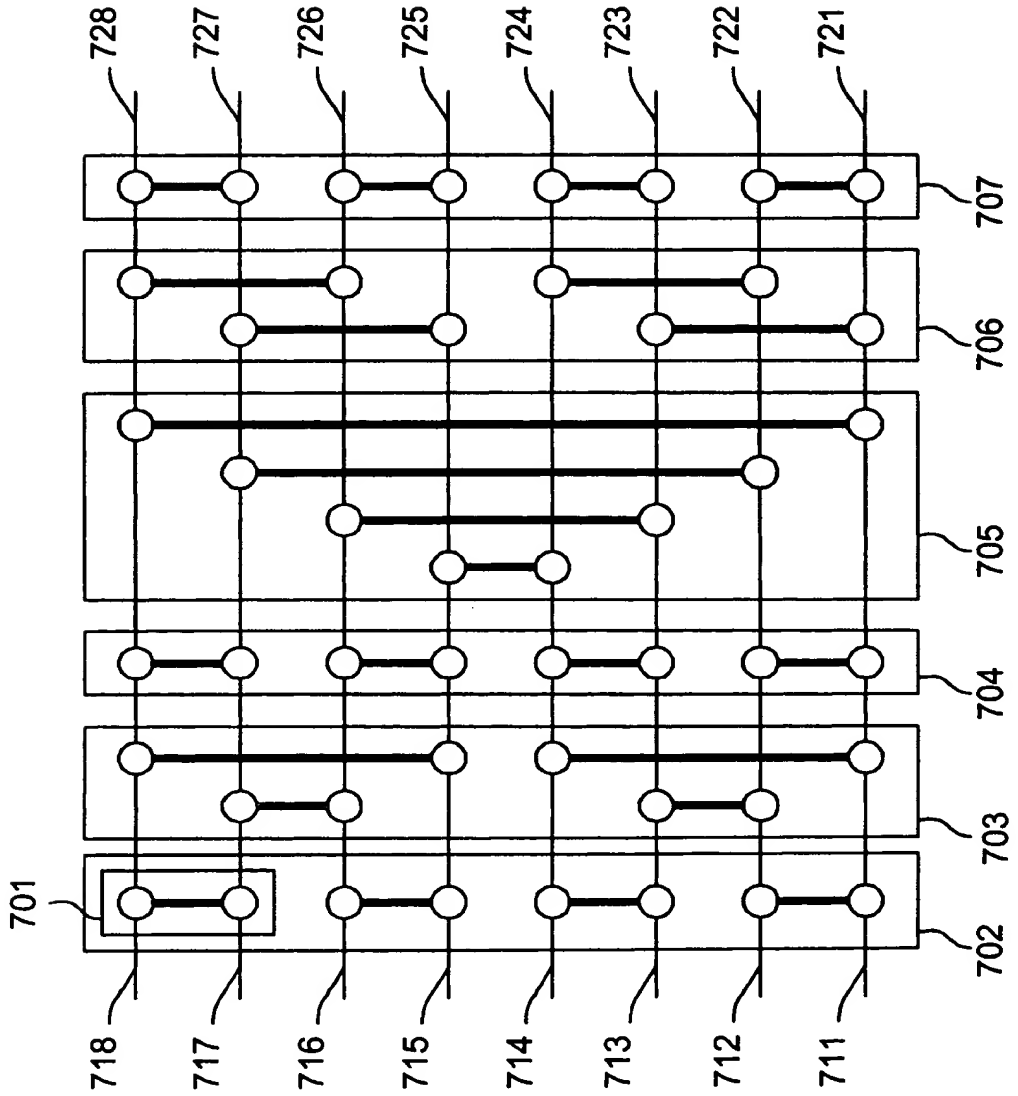


FIG. 11

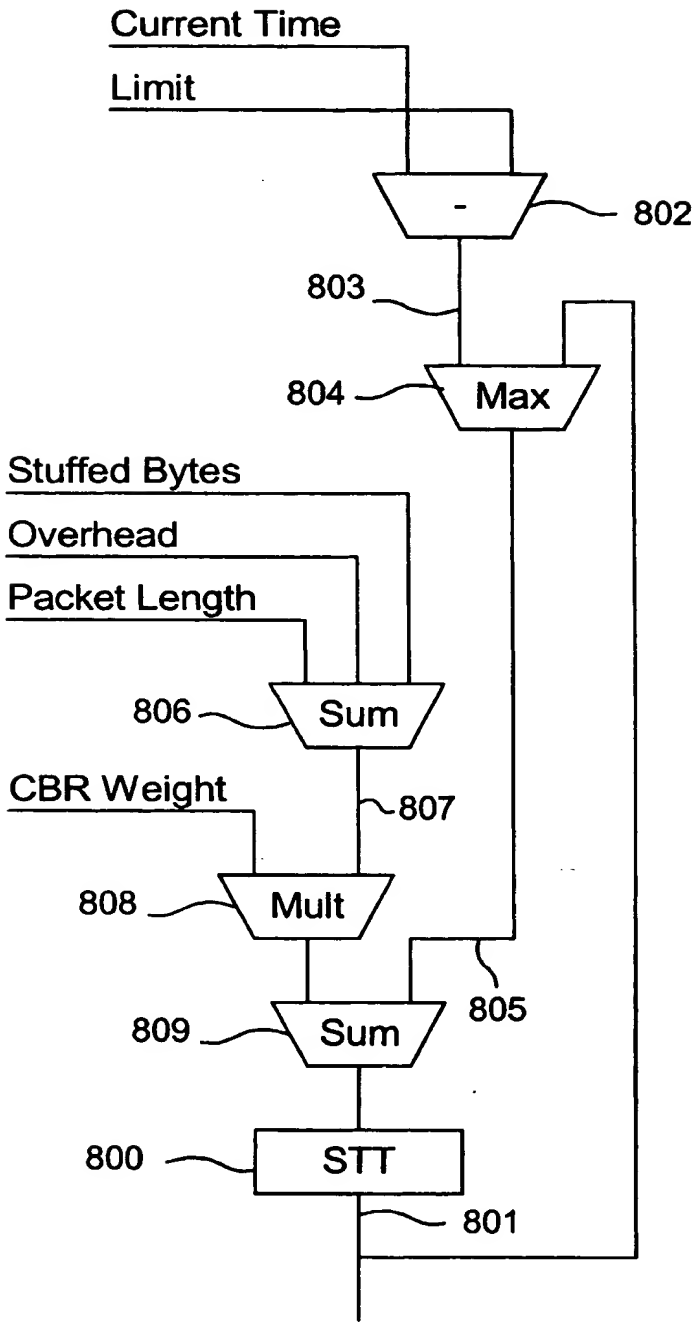

Current Time
Limit
-
802
803
804
Max
Stuffed Bytes
Overhead
Packet Length
806
Sum
CBR Weight
807
808
Mult
805
809
Sum
800
STT
801

FIG. 12

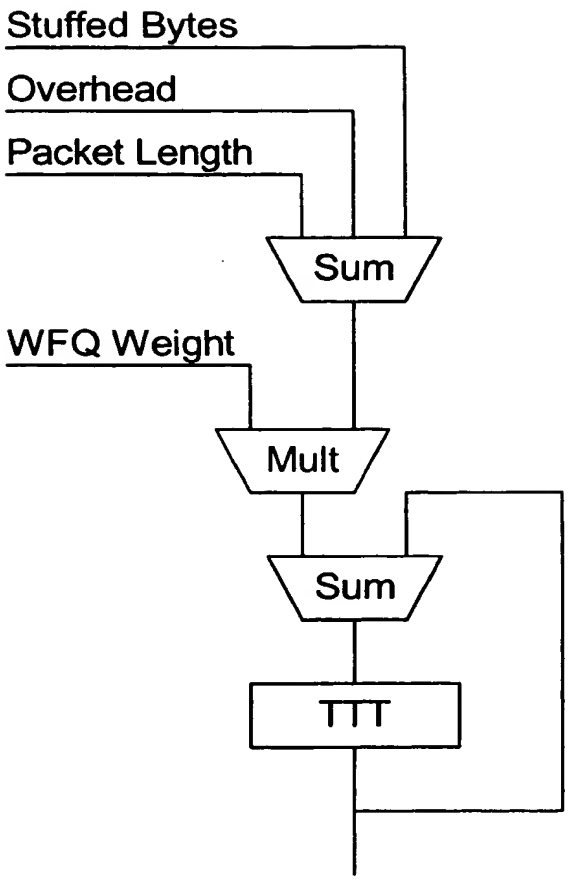


FIG. 13

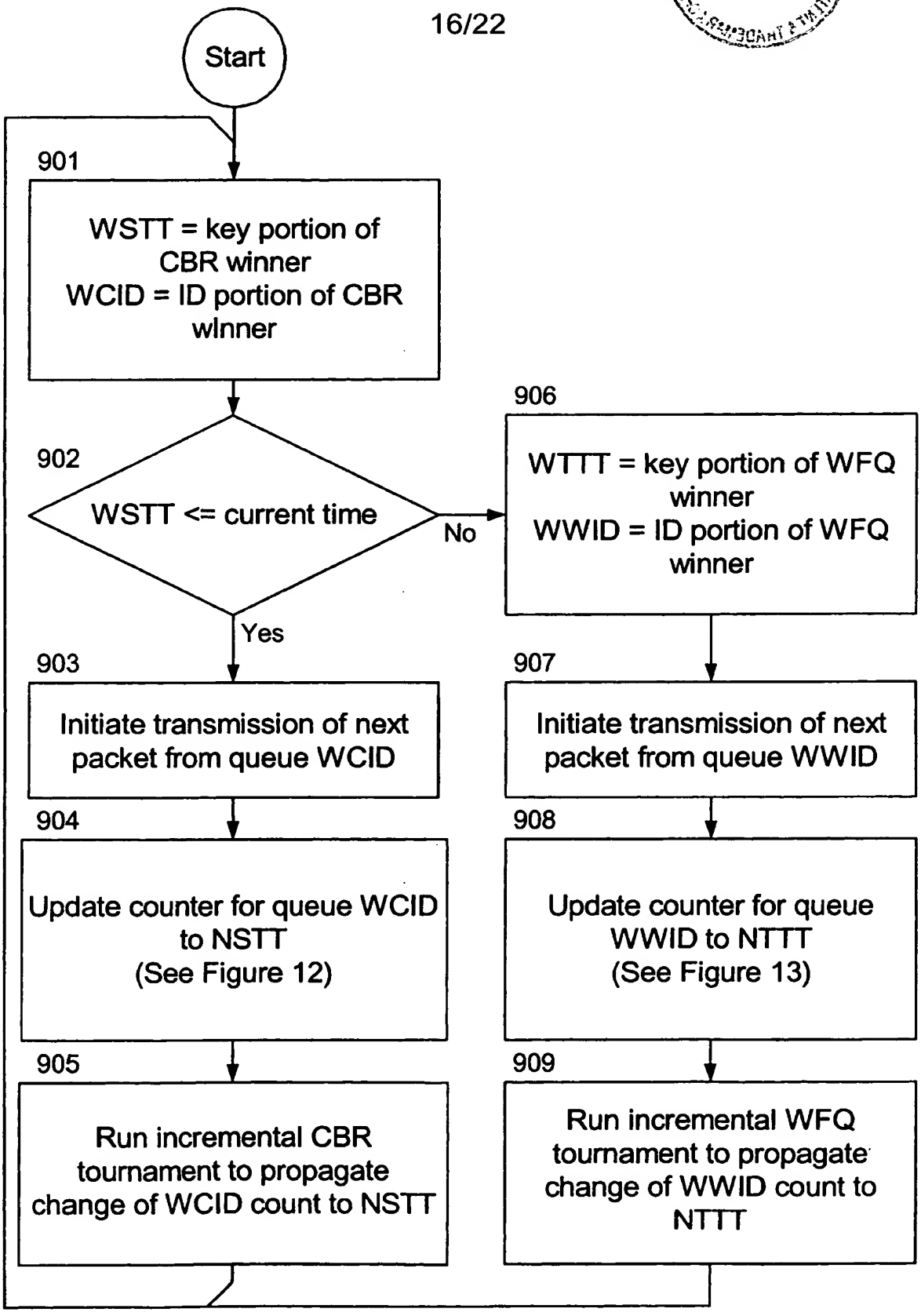

Start
901
WSTT = key portion of CBR winner
WCID = ID portion of CBR winner
902
WSTT <= current time
No
Yes
906
WTTT = key portion of WFQ winner
WWID = ID portion of WFQ winner
903
Initiate transmission of next packet from queue WCID
907
Initiate transmission of next packet from queue WWID
904
Update counter for queue WCID to NSTT
(See Figure 12)
908
Update counter for queue WWID to NTTT
(See Figure 13)
905
Run incremental CBR tournament to propagate change of WCID count to NSTT
909
Run incremental WFQ tournament to propagate change of WWID count to NTTT

FIG. 14

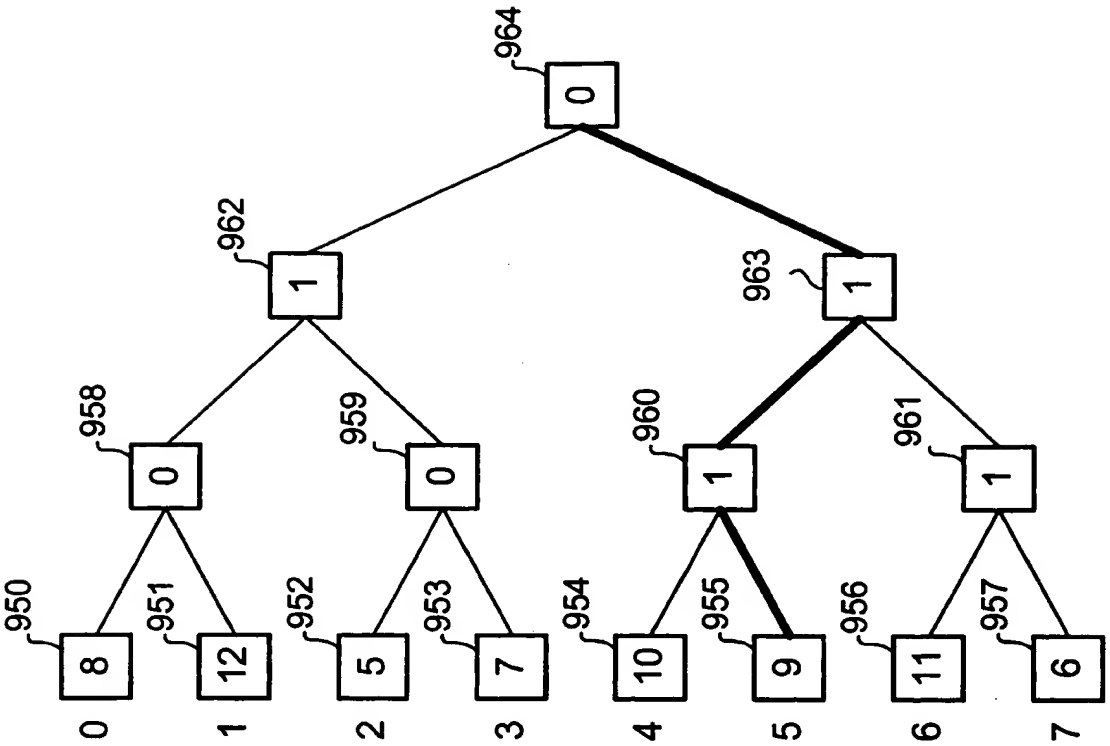


FIG. 16

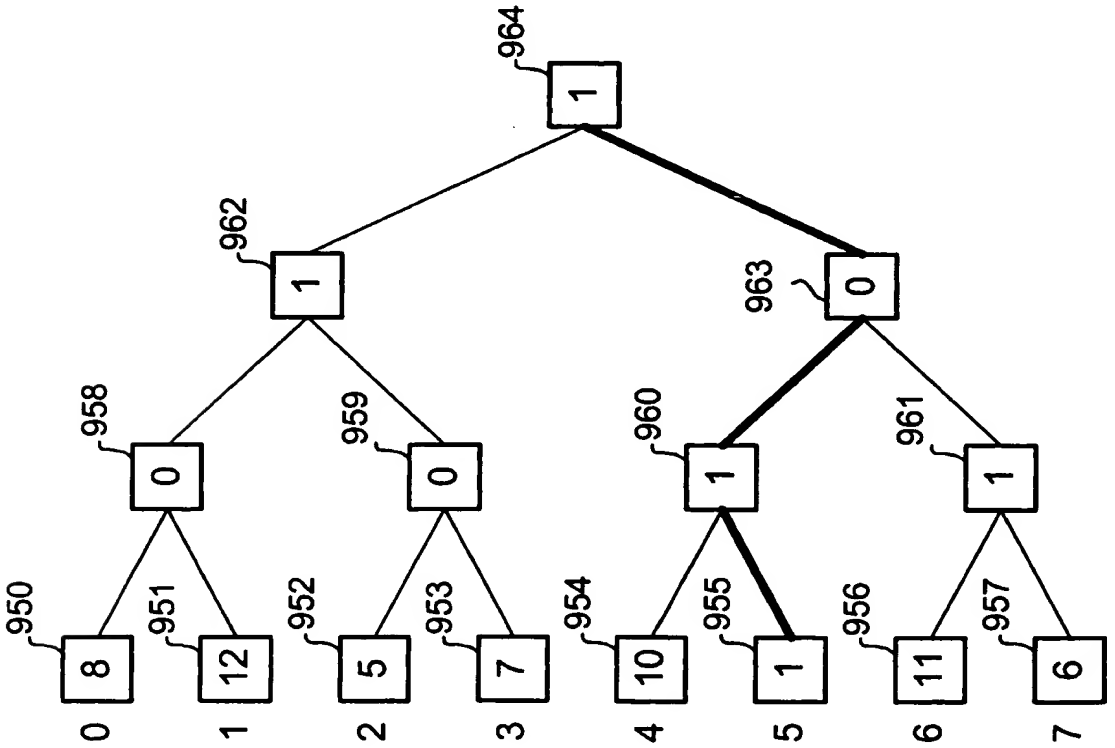


FIG. 15

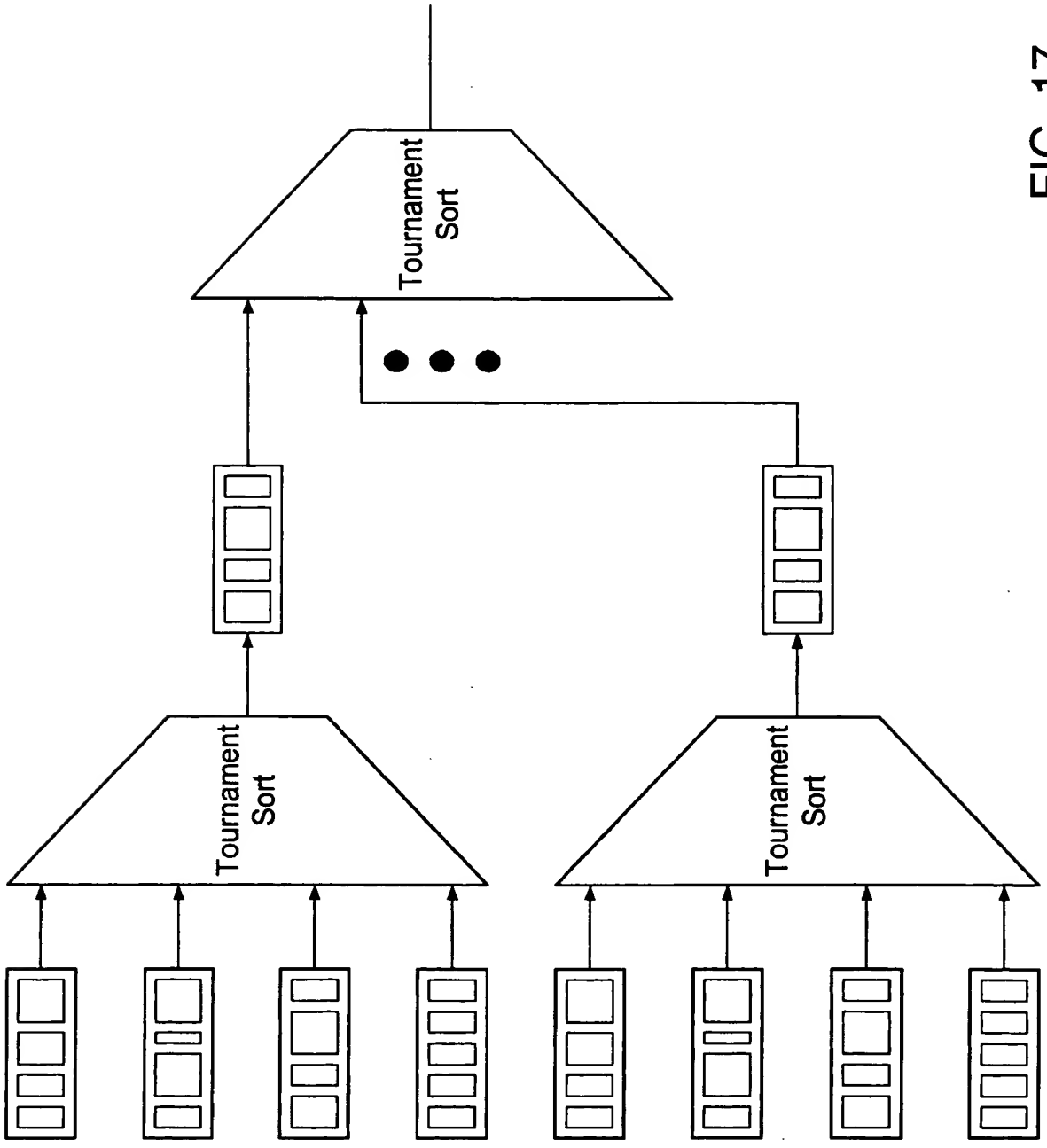


FIG. 17

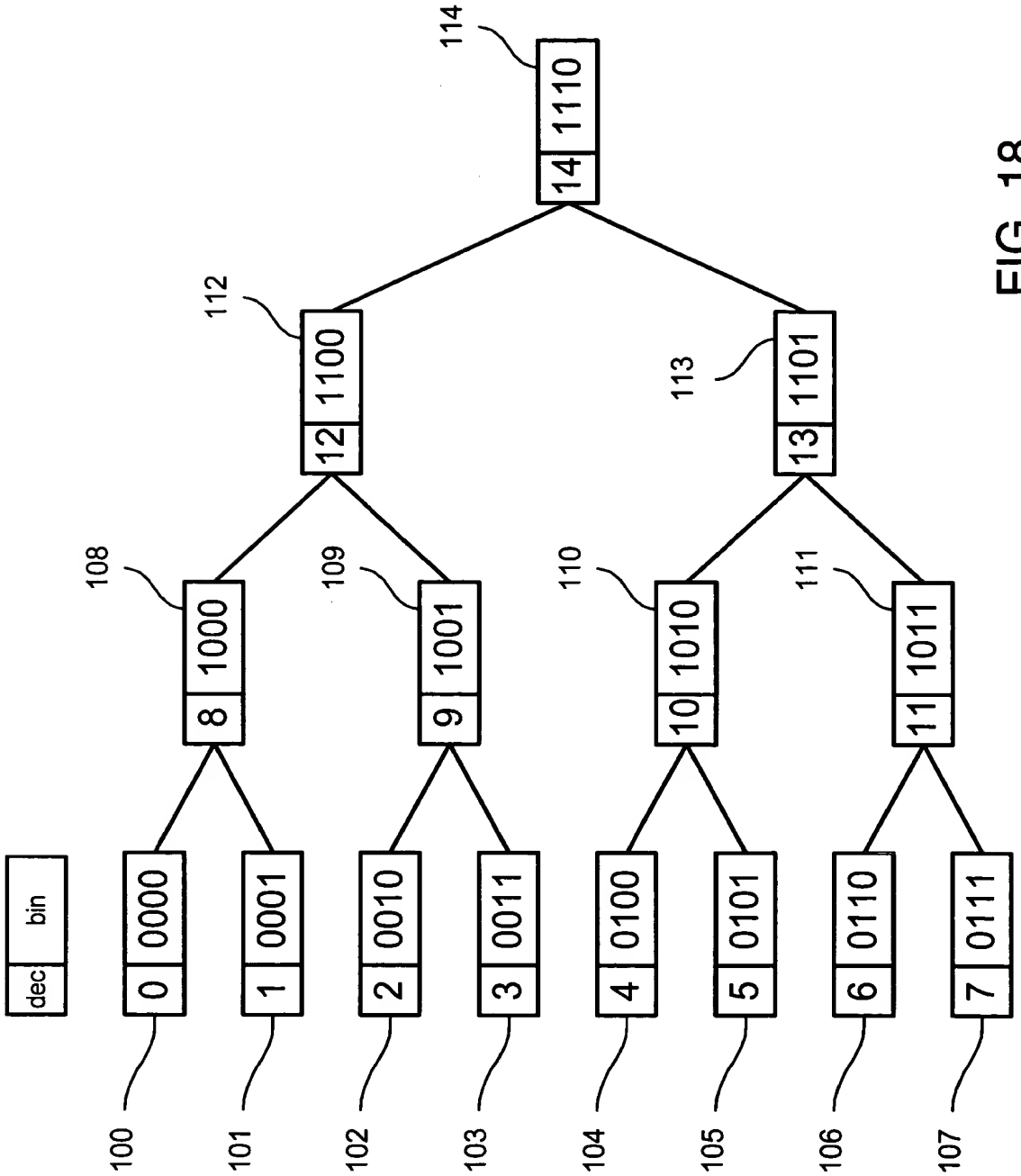

dec
bin
0 0000
1 0001
2 0010
3 0011
4 0100
5 0101
6 0110
7 0111
8 1000
9 1001
10 1010
11 1011
12 1100
13 1101
14 1110
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114

FIG. 18

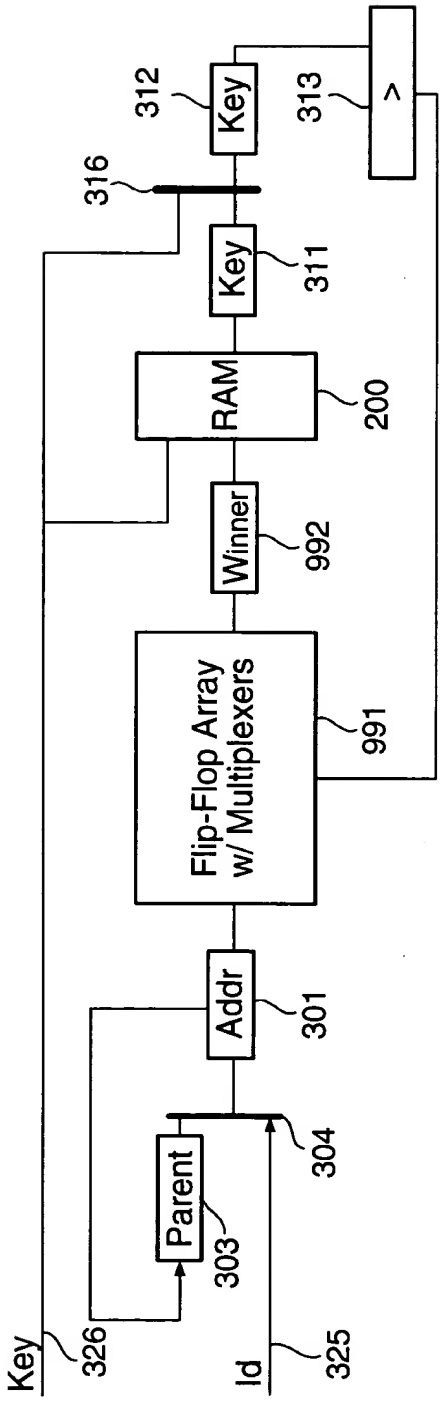

Key
326
Id
325
Parent
303
304
Addr
301
Flip-Flop Array
w/ Multiplexers
991
Winner
992
RAM
200
Key
311
316
Key
312
>
313

FIG. 19

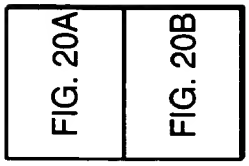


FIG. 20A
FIG. 20B

FIG. 20

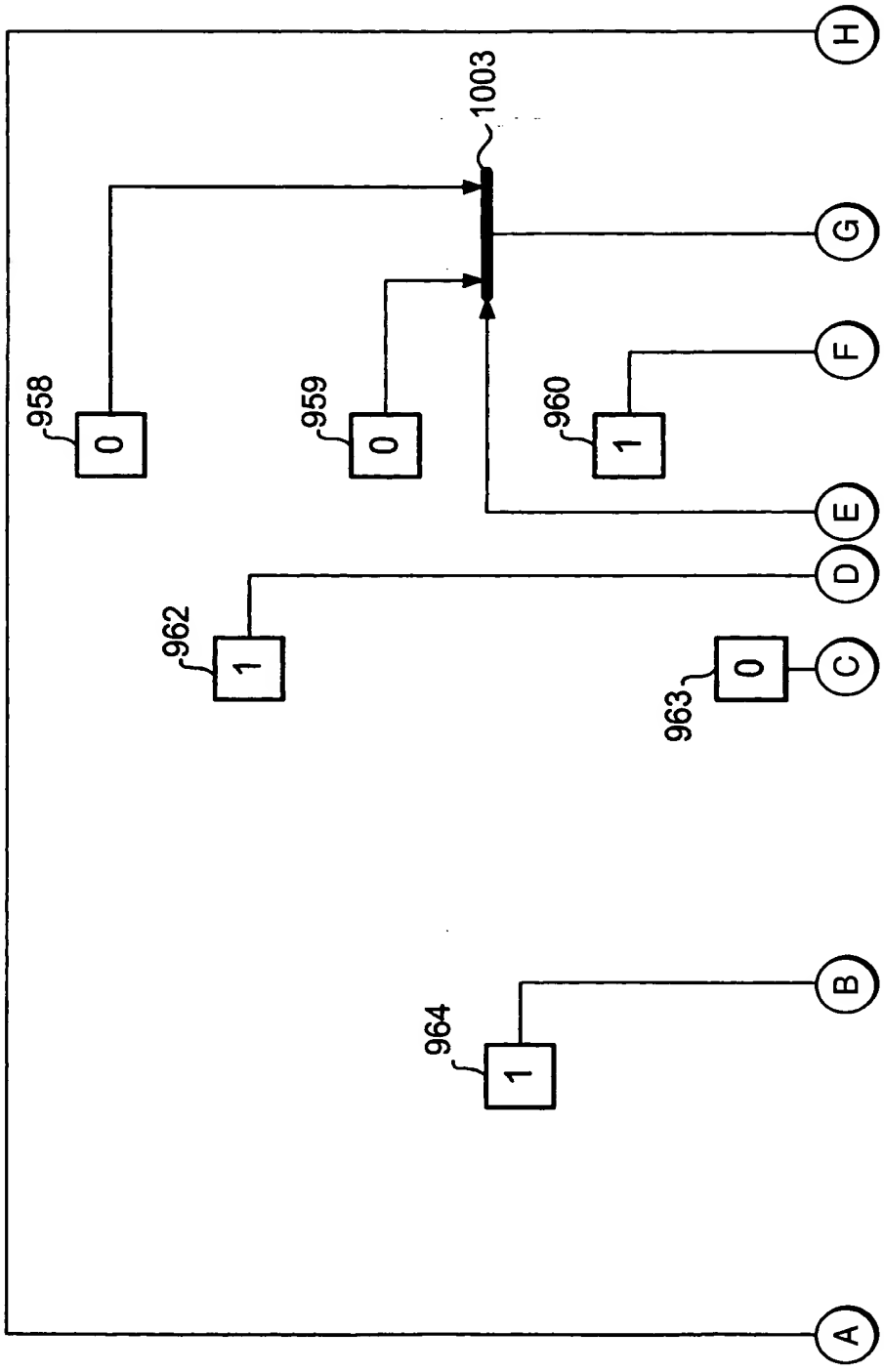


FIG. 20A

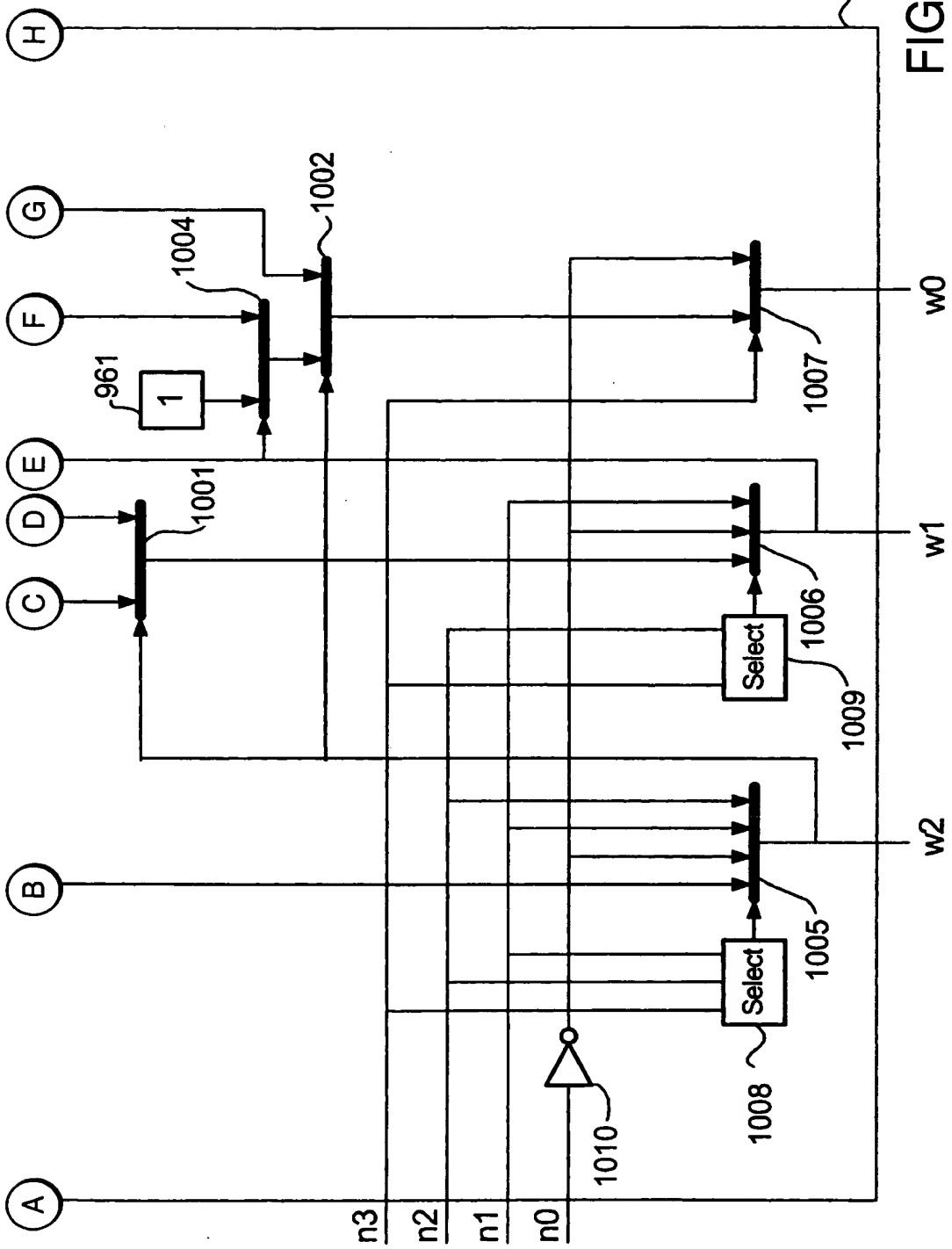

H
G
F
E
D
C
B
A
991
1002
1004
961
1
1001
1007
w0
w1
w2
1006
Select
1009
1005
Select
1008
1010
n3
n2
n1
n0

FIG. 20B